REMARKS

I. General

Claims 1-30 are pending in the current application, and claims 1-30 are rejected. The issues raised in the Office Action mailed June 17, 2004 are:

- Claims 1-8, 13-22, and 26-28 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. US 2002/0166038 to MacLeod (hereinafter *MacLeod*);
- Claims 9-12 and 23-25 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over *MacLeod*; and
- Claims 29-30 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over *MacLeod* in view of by U.S. Patent No. 6,263,445 to Blumenau (hereinafter *Blumenau*).

II. Rejection under 35 U.S.C. § 102 (e) ---*MacLeod*

The Examiner rejected claims 1-8, 13-22, and 26-28 under 35 U.S.C. § 102(e) as being anticipated by *MacLeod*. Applicants respectfully traverse this rejection and assert that the rejected claims are allowable at least for the reasons stated below.

A. Failure to teach every element of the claim

It is well settled that to anticipate a claim, the reference must teach every element of the claim. MPEP § 2131. Applicants respectfully assert that the rejection does not satisfy this requirement.

1. Independent Claims

Claim 1 requires, in part:

> querying said storage device for device identification information;

Claim 21 requires, in part:

> means for querying said storage device for device identification information;

The disclosure of *MacLeod* fails to anticipate claims 1 and 21. The Examiner asserts that the portion of *MacLeod* found at page 2, section 0027, discloses this feature of claims 1 and 21. However, the cited portion of *MacLeod* discloses an entry stored in the I/O virtual

address (IOVA) cache memory that includes an identifying field known as tag bits. (*MacLeod*, page 2, section 0027). *MacLeod* also discloses that an I/O board constructs the tag bits from a portion of a logical address, and the I/O board inserts tag bits as part of the IOVA cache memory entry when updating a cache entry. (*MacLeod*, page 2, section 0027). In addition, *MacLeod* teaches that the I/O board will compare tag bits of the cache memory to a predetermined portion of the logical address when reading a cache entry into the IOVA cache memory. (*MacLeod*, page 2, section 0027). However, the tag bits of *MacLeod* do not correspond to the claimed device identification information, as the tag bits are not related to device identification information. Thus, *MacLeod* fails to disclose all the elements of claims 1 and 21.

2. Dependent Claims

Claims 2-8, 13-20, 22, and 26-28 depend directly or indirectly from their respective base claims 1 and 21 and thereby inherit all of the limitations of their respective base claims. Accordingly, it is respectfully submitted that the dependent claims 2-8, 13-20, 22, and 26-28 are patentable over the 35 U.S.C. § 102 rejection based on *MacLeod*.

III. Rejection under 35 U.S.C. § 103 (a) ---*MacLeod*

The Examiner rejected claims 9-12 and 23-25 under 35 U.S.C. § 103 (a) as being unpatentable over *MacLeod*. Applicants respectfully traverse this rejection and assert that the rejected claims are allowable at least for the reasons stated below.

To establish a prima facie case of obviousness under 35 U.S.C. § 103(a), the prior art cited must teach or suggest all the claim limitations. MPEP § 2143. Applicants respectfully assert that the cited references do not teach or suggest all the claim limitations of claims 9-12 and 23-25, and therefore, the claims are not obvious under 35 U.S.C. § 103(a).

A. Failure to teach or suggest all claim limitations

Base claims 1 and 21 are patentable due to the deficiencies of *MacLeod* as discussed above. The Examiner's assertion of obviousness is not relied upon as disclosing these deficiencies. Claims 9-12 and 23-25 depend indirectly from base claims 1 and 21 respectively, and thus, inherit all limitations of their respective base claims 1 and 21. Therefore, *MacLeod* and the Examiner's assertion of obviousness fails to teach all the

elements of claims 9-12 and 23-25, and, thus, claims 9-12 and 23-25 are not obvious under 35 U.S.C. § 103(a). Thus, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection for claims 9-12 and 23-25 be withdrawn.

IV. Rejection under 35 U.S.C. § 103 (a) ---*MacLeod & Blumenau*

The Examiner rejected claims 29 and 30 under 35 U.S.C. § 103 (a) as being unpatentable over *MacLeod* in view of *Blumenau*. Applicants respectfully traverse this rejection and assert that the rejected claims are allowable at least for the reasons stated below.

To establish a prima facie case of obviousness under 35 U.S.C. § 103(a), the prior art cited must teach or suggest all the claim limitations. MPEP § 2143. Applicants respectfully assert that the cited references do not teach or suggest all the claim limitations of claims 29 and 30, and therefore, the claims are not obvious under 35 U.S.C. § 103(a).

A. Failure to teach or suggest all claim limitations

1. Independent Claim

Claim 29

Claim 29 requires, in part:

> wherein each of said at least one host agent process is operable to query said at least one storage device embedded in or coupled to said host system on which said host agent process resides for device identification information...

The cited references fail to teach or suggest this feature of claim 29. In rejecting claim 29, the Examiner relies on the rejections made with respect to claims 1 and 21. However, as discussed above, *MacLeod* discloses an entry stored in the I/O virtual address (IOVA) cache memory that includes an identifying field known as tag bits that are constructed by an I/O board from a portion of a logical address, and the I/O board inserts tag bits as part of the IOVA cache memory entry when updating a cache entry. (*MacLeod*, page 2, section 0027). In addition, *MacLeod* teaches that the I/O board will compare tag bits of the cache memory to a predetermined portion of the logical address when reading a cache entry into the IOVA cache memory. (*MacLeod*, page 2, section 0027). However, as discussed above with respect to claims 1 and 21, the tag bits of *MacLeod* do not correspond to the

claimed device identification information, as the tag bits are not related to device identification information. Furthermore, *Blumenau* is not relied upon as disclosing these limitations. (Office Action, page 9). Thus, *Blumenau* fails to cure the deficiencies of *MacLeod*. As such, the combination of *MacLeod* and *Blumenau* fails to teach all the elements of claim 29, and thus, claim 29 is not obvious under 35 U.S.C. § 103(a). Therefore, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection for claim 29 be withdrawn.

2. Dependent Claim

Claim 30 depends directly from the respective base claim 29 and thereby inherits all of the limitations of the respective base claim. Accordingly, it is respectfully submitted that dependent claim 30 is patentable over the 35 U.S.C. § 103(a) rejection based on *MacLeod* in view of *Blumenau*.

V. Summary

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Applicants believe no fee is due with this response. However, if a fee is due, please charge Deposit Account No. 08-2025, under Order No. 10004559-1 from which the undersigned is authorized to draw.

I hereby certify that this correspondence is being deposited with the United States Postal Service Express Mail Label EV482734647US in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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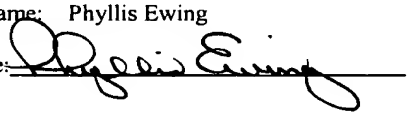
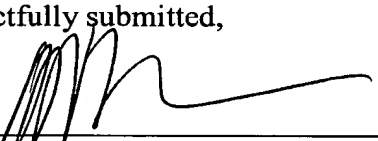
Signature: 

Respectfully submitted,

By: 

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